Taming Emerging Devices' Variation and Reliability Challenges with Architectural and System Solutions [Invited]

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Abstract—**Emerging devices are promising alternatives to traditional CMOS technologies as proposed in various solutions for future computation and communication systems. However, such devices often suffer from significant variations and relatively poor reliability. To address such limitations for their broader adoption, novel techniques at circuit, architecture, and system levels could help alleviate the device variation and reliability challenges. In this paper, we illustrate the effectiveness of such techniques in three distinct application domains, namely non-volatile memories, flexible electronics, and silicon photonics-enabled optical interconnects.**

I. INTRODUCTION

The CMOS integrated circuits have experienced enormous success in the past few decades through continuous technology scaling, which shaped today's industrial and consumer electronics. However, with the scaling rate gradually slowing down and to eventually hit the atomistic and quantum mechanical physics boundaries [1], traditional CMOS technologies may prove inadequate to accommodate the rapid growth of future computation- and communication-hungry applications, as well as new sensing applications which require innovative forms of interfaces to humans. Alternative material and devices are being actively investigated to assist, and potentially replace, traditional silicon electronics in emerging application domains such as next-generation non-volatile memories, flexible electronics, optical interconnects, spintronics, quantum computing, etc. Despite promising results demonstrated by theoretical derivations and prototypes, emerging devices often suffer from significant process variations and reliability issues due to immature fabrication techniques. Such limitations must be tackled before any broad adoption can take place. In addition to the efforts put into device optimization and process control, innovative techniques applied at circuit, architecture, and system levels could also help alleviate the variation and reliability challenges.

NAND flash, for instance, is a non-volatile memory (NVM) technology that successfully tackled these limitations and now it is virtually everywhere, from cheap USB thumb drives to mobile devices and enterprise storage applications. Among architectural solutions, memory cell disturbs while reading and writing adjacent cells was reduced by changing the conventional half-bit-line (HBL) architecture to the all-bit-line (ABL) architecture, which reduced by half the stress on the bit lines. Low reliability margins are addressed with stronger error correcting codes, as well as with system-level algorithms to tune the memory chip for a specific type of application (e.g. read- versus write-intensive applications). The premature death of memory blocks due to the limited endurance of the memory cells (i.e. the maximum number of times a cell can be reliably written into) is prevented with wear-leveling algorithms, that aim to distribute memory writes as evenly as possible. An undesired effect of this is that the same logical data may be present in more that one physical location in the memory, a phenomenon known as write amplification. This last problem is typically overcome by over-provisioning the memory, i.e., by providing extra physical storage capacity that is not visible to the user.

In the rest of this paper, we use three specific examples, namely non-volatile memories, flexible electronics, and silicon photonics-enabled optical interconnects, to illustrate the recent progress of circuit-, architecture-, and system-level techniques applied to emerging devices and their effectiveness in variation and reliability management.

II. NON-VOLATILE MEMORIES

A. Introduction

The need for larger, faster, and lower-power memories has been addressed so far by aggressive technology downscaling and operating voltage reduction. Dynamic random-access memory (DRAM) and NAND flash, as the current prominent technologies for main memory and storage, respectively, have been following this trend. However, the ever-increasing performance gap between them has rendered a memory system solely based on these two technologies inadequate in the long term [2]. Resistive random-access memory (ReRAM) based on two-terminal resistance switching memristive devices is a promising contender to fill such gap. ReRAM, a non-volatile memory (NVM) technology, offers memory densities that are comparable to those of NAND flash, and fast random accesses that are comparable to those of DRAM, effectively offering the advantages of both technologies [3].

B. Memristive Devices and ReRAM Architectures

The main memory element in a ReRAM unit cell is the memristor, whose characteristic feature is the so-called pinched hysteresis loop in its current-voltage (I-V) plane [4], as shown in Fig. 1(a). Due to its structural simplicity (two electrodes sandwiching a thin oxide layer, as shown in Fig. 1(b)), an array of memristors can be organized in a crossbar fashion, in which at each cross-point, a memristor is formed (Fig. 1(c)). This is known as the 1TnR architecture, and it is the preferred ReRAM architecture from the density point of view, as every electrode is connected to n memristors and one transistor is

needed for accessing each electrode for reading from or writing to any of the n memristors. Integrating large memristive crossbars arrays, however, have proven challenging due to the high power consumption that originates from leakage currents (known as the sneak-path problem), and the large device-to-device (D2D) and cycle-to-cycle (C2C) variations of memristors. The D2D and C2C variations are the results of the intrinsically stochastic resistance switching mechanism of the memristors [5], [6], whereas the sneak-path problem is caused by the parasitic currents that result while accessing a single device in 1TnR ReRAM crossbars [7], as depicted in Fig. 1(d).

As a memory element, the memristor in a ReRAM cell can be reversibly switched between a high-resistance state (HRS) and a low-resistance state (LRS) by means of an external voltage applied across its terminals. Logic '1' is typically represented by setting its memristor into an LRS, whereas a logic '0' is represented by setting it into an HRS. The state of a memory cell is then determined by applying a small read voltage across its memristor and comparing the resulting current with a reference current. This is the traditional way of reading the state of a ReRAM cell, and we call it a "resistance-based current sensing" approach. A major issue with this approach is that the intrinsic D2D and C2C variations in memristors manifest into a large distribution of the LRS and HRS resistances, making it difficult to define a reference to differentiate a logic '1' from a logic '0', as experimentally evidenced with the four consecutive write cycles of three pairs of memristors in Fig. 2 and its inset.

C. ReRAM based on Ratioed Memristors

In [8] we report our approach to mitigate the sneak-path problem and significantly reduce the D2D and C2C variations of memristors. It consists on a ReRAM architecture and a memory cell called "H3 cell" comprised of two serially-

Fig. 2. Four consecutive current-voltage write cycles for three pairs of titanium oxide-based devices using a traditional resistance-based current sensing approach, and a zoomed-in view of the read region.

Fig. 3. Proposed H3 cell and its array architecture. An H3 cell is formed by two anti-serially connected bipolar memristors (left and right) and a minimum-sized field effect transistor (mFET).
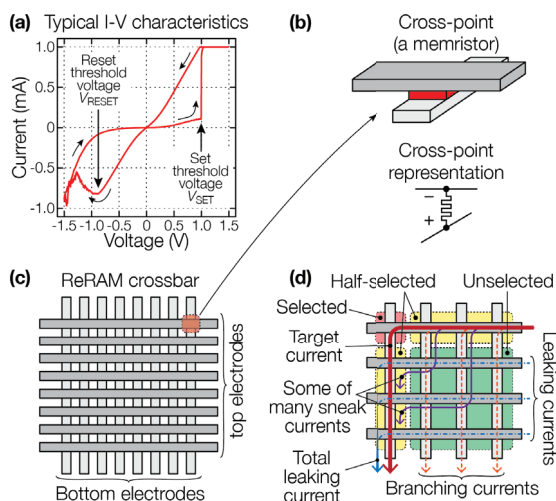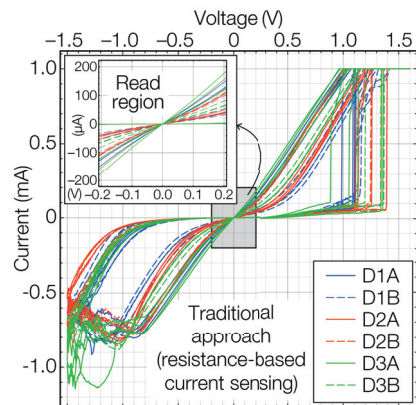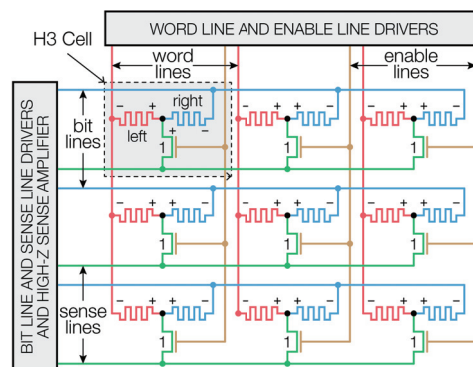

Fig. 1. (a) Typical I-V characteristics for a bipolar titanium oxide-based device. (b) Symbol and simplified structure of a memristor. (c) A crossbar array of ReRAM cells. (d) Sneak-path and other parasitic currents in a ReRAM crossbar.
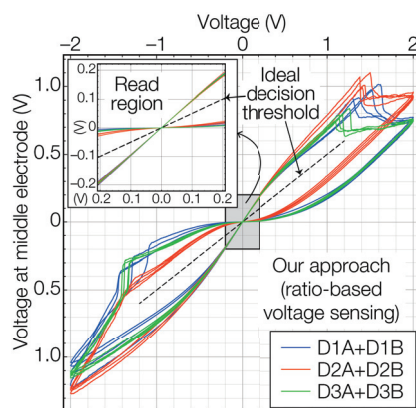

Fig. 4. Four consecutive voltage-voltage write cycles of the same pairs of devices of Fig. 2 using our ratio-based voltage sensing approach, and a zoomed-in view of the read region.

connected memristors (*left* and *right*) and a minimum-sized transistor (*mFET*), as shown in Fig. 3. The mFET, which is connected to the midpoint between the two series-connected memristors, is used to sense the voltage for reading the state of the cell.

An H3 cell's logic '1' is encoded with the left memristor in an HRS, and the right memristor in an LRS (HRS|LRS configuration). Similarly, an LRS|HRS configuration represents a logic '0'. The key idea is that we retrieve the state of an H3 cell based on the *ratio of resistances* of the left and right memristors. Specifically, the state of an H3 cell is read by (1) enabling its mFET, (2) applying a read voltage V_R (which is small and non-destructive) across the left and right memristors, and (3) sensing the voltage V_S at the internal electrode with a high-impedance sense amplifier at the end of the sense line. If $V_S > V_R/2$, the H3 cell stores a logic '1', otherwise (i.e. $V_S < V_R/2$), it stores a logic '0'. We call this a "ratio-based voltage sensing" approach, in contrast to the traditional resistance-based current sensing approach. Note that for a sufficiently large HRS/LRS resistance ratio, which is the case for most memristive materials, the output of the voltage divider that is formed by the left and right memristors will be very close to either the reference ground potential for logic '0', or V_R for logic '1'.

Encoding the state of an H3 cell as a voltage divider results in narrower distributions for both logic 0 and 1 states than those whose states are directly based on memristors resistances. This point is illustrated by Fig. 4 and its inset, in which the same three pairs of devices of Fig. 2 are cycled but now as a pair of serially-connected devices. In contrast to the current-voltage (I-V) plot of Fig. 2, the data shown in Fig. 4 for the proposed ratio-based approach uses a voltage-voltage (V-V) plot, in which the x-axis is the applied voltage across the *left* and *right* memristors, and the y-axis is the voltage measured at the midpoint between these two memristors.

There are several benefits of our ratio-based voltage sensing approach when compared to the traditional resistance-based current sensing approach:

1) For a given set of LRS and HRS resistance distributions, our approach results in much tighter state distributions, which significantly reduces the error rate of the encoded data.
2) The ideal voltage reference, $V_R/2$, for reading an H3 cell depends solely on the read voltage V_R, and not on the actual resistance of the memristors, as is the case for the resistance-based approach.
3) Such an ideal voltage reference need not be changed with the aging of the devices, contrasting to the optimal threshold in a resistance-based approach which is device-dependent and it needs to cope with the memristor's possible resistance drift due to aging and temperature variations [9].
4) The state of an H3 cell is bounded in the (0, V_R) range, compared to an unbounded memristor resistance that can be arbitrarily high or low.
5) An H3 cell-based ReRAM crossbar is sneak-path-free since the stack of the serially-connected memristors in an

Device Type (TFT)	Amorphous Si	Metal-Oxide	SAM Organic	Carbon Nanotube
Process Temperature	$\sim 250°C$	$\sim 150°C$	$\sim 100°C$	Room temp.
Process Technology	Lithography	Lithography/ Roll-to-roll	Shadow mask	Solution/ shadow mask/ roll-to-roll
Feature Size (μm)	~ 8	$\sim 2\text{-}5$	~ 50	$\sim 2\text{-}5$
Stable Device Type	N-type	N-type	P-type	P-type
Supply Voltage (V)	~ 20	~ 5	~ 2	$\sim 1\text{-}2$
Mobility (cm^2/Vs)	~ 1	~ 10	~ 0.5	~ 25

H3 cell is seen as a high resistance device, which greatly reduces the parasitic currents described in Fig. 1(d).

III. FLEXIBLE ELECTRONICS

A. Introduction

Flexible electronics is emerging as an alternative to conventional silicon electronics for applications such as wearable sensors, artificial skin, medical patches, bendable displays, foldable solar cells and disposable RFID tags [10] [11]. Fig. 5(a) and (b) show a test sample of a recent Pseudo-CMOS logic circuit with carbon nanotube thin film transistors (CNT TFTs) on a 1 μm thick polymer substrate [12]. Unlike conventional silicon electronics that need sophisticated billion-dollar foundry for manufacturing, flexible electronic circuits can be fabricated on thin and conformable substrates such as plastic films, with low-cost high-throughput manufacturing methods such as ink-jet printing and roll-to-roll imprinting. The time-to-market, as well as manufacturing cost, can thus be significantly reduced. Its flexible form factor also enables innovative designs for consumer electronics and biomedical applications [13] [14].

There exist several challenges before flexible electronics can be broadly employed for next-generation wearable and IoT products. Due to material properties, TFTs are usually mono-type, either p- or n-type only, devices [12], as shown in Table. I. Making air-stable complementary TFT circuits is quite challenging and often requires heterogeneous process integration of two different TFT technologies. Existing CMOS design methodologies for silicon electronics, therefore, cannot be directly applied to designing flexible electronics. Other factors such as high supply voltages and large process variations also make designing large-scale TFT circuits a significant challenge.

B. Robust Pseudo-CMOS Circuits

Pseudo-CMOS is a design style proposed to address challenges of TFT circuit design based on mono-type devices [10], which has been proven a robust design style for flexible digital,
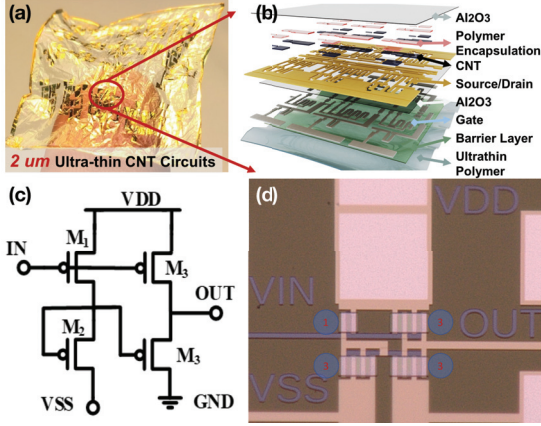
Fig. 5. (a)&(b). Ultra-thin CNT TFT circuits [15]; (c)&(d), Pseudo-CMOS inverter and die photo.

analog, and power circuits. Compared to conventional mono-type digital design styles, such as the diode-load or resistive-load designs, Pseudo-CMOS offers better noise margin and provides post-fabrication tunability at the cost of an additional power rail V_{SS}. Both Pseudo-CMOS inverter's schematic and die-photo are shown in Figs. 5(c) and (d), which consists of three power rails, V_{DD}, V_{SS} and *GND*, and four transistors M_{1-4}. Typically, M_1:M_2:M_3:M_4 is set to be 1:3:3:3 to guarantee a good noise margin, as illustrated in Fig. 5(d).

C. Post-tuning for Variation Suppression

Variations of flexible electronics could be large ($\sim$10%-30%). For instance, we characterized CNT TFTs' key parameters, such as V_{th} and mobility μ with 56 CNT TFTs cross over a 4 inch wafer. All transfer curves of 56 TFTs are plotted together in Fig. 6(a) and extracted statistical information of V_{th} and mobility μ are presented in Fig. 6(b) and (c). Pseudo-CMOS design is proposed to address such large variations through post-tuning capability. The post-tuning is illustrated in Fig. 6(d), where the VSS changes from 0 V to -3 V with a VDD = 2 V. Accordingly, the voltage transfer curves' variations reduced from $\sim$0.5 V to $\sim$0.25 V ($\sim$50%) and also the voltage gain increased from $\sim$5-30 to $\sim$200-300 (>10x). Such a post-tuning capability is one of the key reasons that Pseudo-CMOS has been widely recognized as a robust design style for mono-type TFT circuits design, although it is at the cost of an additional power supply, extra area and interconnects [10].

D. Flexible Hybrid Electronics for Human Sensing System

Based on the robust Pseudo-CMOS design of CNT TFTs, we've successfully prototyped an ultra-thin *active electrode* which integrates a 2-μm CNT TFT amplifier with the electrocardiogram (ECG) capacitive sensor [15]. The ultra-thin amplifier provides low-noise signal amplification for the ECG signal, is fully integrated with the ECG sensor, and thus greatly boosts the signal integrity. Our prototyped *active electrode* shows great potential for continuous, long-term, and high-quality human-machine interfaces with unprecedented comfort
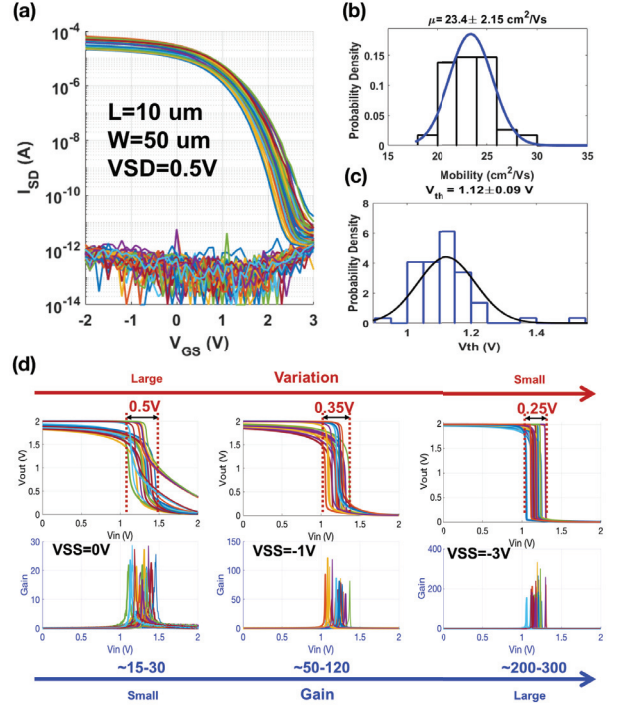

Fig. 6. (a). Transfer characteristics of 56 CNT TFTs with L=10um and W=50 um on a 4 inch wafer; (b)&(c). Extracted mobility and threshold voltage (V_{th}) based on traditional CMOS linear region model; (d). post-tuning of Pseudo-CMOS inverters.

and wearability for the users. Furthermore, through heterogeneous integration of flexible devices and thinned silicon chips, known as flexible hybrid electronics (FHE), we can bring low-cost sensing and high-performance computing to a much wider range of applications, such as wearables, IoT sensing nodes, and various human-machine interfaces [12].

IV. SILICON PHOTONICS OPTICAL INTERCONNECTS

A. Introduction

Dense wavelength division multiplexing (DWDM) optical interconnects are considered promising to accommodate traffic-intensive applications in future high-performance computing systems. Silicon photonics is emerging as a cost-effective and scalable implementation by taking advantage of large-scale CMOS-compatible integration [16]. Recent innovations in quantum-dot (QD) comb lasers and microring resonators have enabled concurrent DWDM with a compact footprint [17]. Fig. 7 illustrates the typical architecture of a microring-ring based transceiver (TRx) link.

Microring resonators are highly wavelength-selective devices which can be used to modulate or filter optical signals at their resonance wavelengths [18]. In microring-based optical links, the microring radii are designed to provide a set of discrete resonance wavelengths with a constant channel spacing, each aligned with a carrier wavelength provided by the laser. Nevertheless, manufacture imperfections of microring devices result in significant deviation of the resonance wavelengths. Shown in Fig. 8 is the measured transmission spectra of one of
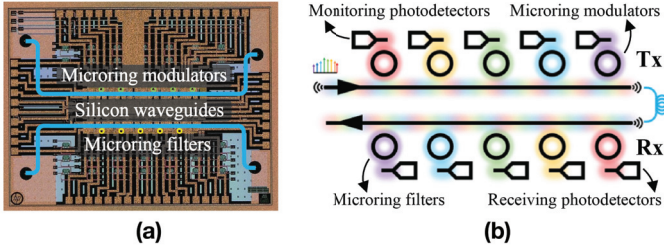
Fig. 7. (a) Microscopic image and (b) architecture illustration of a microring-based transceiver.

Fig. 9. Illustration of microring tuning distance (a) without and (b) with sub-channel redundant comb lines.

our fabricated transceivers, and the variation characterization of resonance wavelengths across 45 measured devices. Active post-fabrication tuning of the resonance wavelengths costs non-trivial energy consumption [19] which must be mitigated through architectural and system solutions.

Taking advantage of the periodicity of the microring transmission spectrum, a cyclic tuning scheme has been proposed to reduce the average tuning cost, often referred to as *channel shuffling* or *channel remapping* [20], [21]. In this section, we briefly review three other techniques that can be applied on top to further reduce the microring tuning cost and thus improve the overall energy efficiency of the optical link.

B. Sub-Channel Redundancies

For multi-channel microring-based optical transceivers, sub-channel redundant microrings can be fabricated, whose resonance wavelengths are designed to be evenly placed between two nominal channels, as we proposed in [22]. To rectify the variations of resonance wavelengths, either the nominal microring or one of the spares is selected and tuned towards the carrier wavelength, so that the tuning distance is minimized. Despite that the resonance wavelengths of the non-selected microrings need to be slightly tuned away from the carrier wavelength to avoid excessive crosstalk, the exploration of such trade-off revealed the opportunity for significant savings of overall energy consumption.

In [23] we proposed another solution that utilizes QD comb lasers with a comb spacing smaller than the microring channel spacing, and thus redundant laser comb lines are available between adjacent channels (Fig. 9). Despite some energy consumed by unused laser comb lines, the energy saved

from microring tuning brings considerable improvement to the overall energy efficiency of the transceiver link.

C. Bidirectional Microring Tuning

For carrier-injection microring resonators, the electro-optic (EO) and thermal-optic (TO) effects shift the resonance wavelengths in opposite directions [24], which provides such devices with an inherent capability of bidirectional tuning. Despite better energy efficiency as compared to thermal tuning, electrical tuning is seldom adopted for it often results in degradations of extinction ratios (ER) and quality factors (Q) of the microring transmission spectra [25]. However, our bidirectional tuning scheme proposed in [26] shows that if the required tuning distance is small and thus the degradations of ER and Q are limited, such degradations can be compensated by the increase of laser power to maintain transmission quality, if the overall power consumption of the transceiver is still lower than that of thermal-only tuning. As shown in Fig. 10, for commonly used per-channel data rates in the range of 5∼10 Gb/s, the bidirectional tuning strategy (the right bar of each 3-bar group) results in 32%∼53% savings of overall energy per bit of the transceiver link compared to all-thermal tuning (the middle bar).

D. Optimal Pairing of Transceivers

In [27] we exploited wafer-level process variations of the microring resonators to further reduce the average tuning
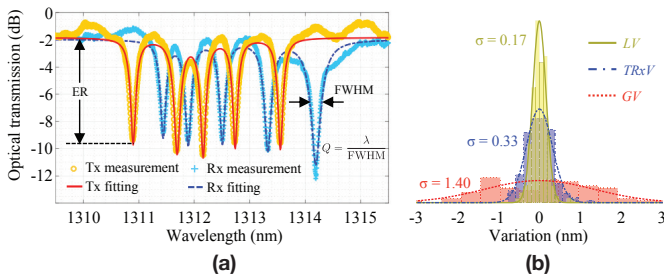

Fig. 8. (a) Measured and fitted spectra of a 5-channel transceiver, where FWHM: full width at half maximum. (b) Variation characterization for resonance wavelengths.
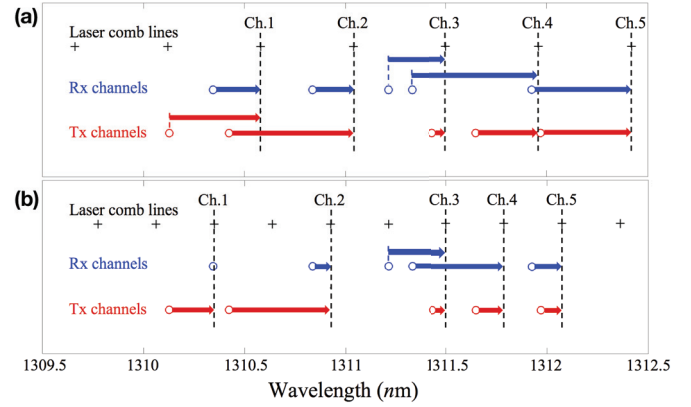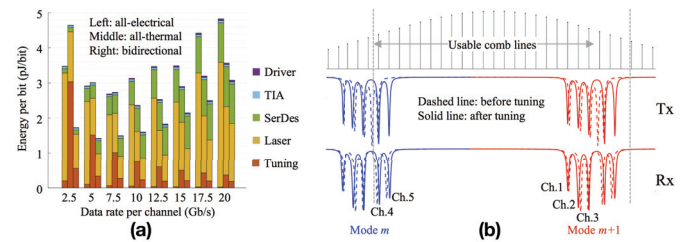

Fig. 10. (a) Evaluation of bidirectional tuning on measured data; and (b) optimal tuning scheme computed for an exemplar transceiver where electrical tuning opportunities are identified for channel 1 and 2.
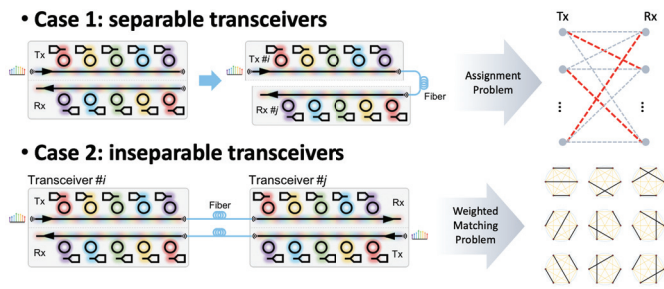
Fig. 11. Optimal pairing problem formulation.

power when a large number of transceiver devices are available. In such a case, a device does not have to pair with its neighboring one in order to form a communication link. Instead, a mix-and-match of all devices available on the wafer may minimize the average tuning power required for each pair. Depending on whether a transceiver can be further diced apart as a transmitter (Tx) and a receiver (Rx), the optimal pairing is formulated as either an assignment problem or a weighted matching problem (Fig. 11), solved by the Hungarian Algorithm [28] or a simulated annealing-based algorithm, respectively. We demonstrated that the optimal pairing of transceiver devices not only reduces the average tuning cost for each pair significantly, but also reduces the variance of tuning costs across different pairs, which is favorable in terms of product uniformity as well.

V. Conclusion

In this paper, we briefly reviewed three fast evolving application domains, namely non-volatile memories, flexible electronics, and silicon photonics-enabled optical interconnects, where circuit-, architecture-, and system-level innovations help alleviate the variation and reliability challenges faced by imperfect devices. Smart applications of such techniques can greatly promote the broad adoption of emerging technologies, especially when improvements in device fabrication and process control lag behind the imminent need. Techniques that target thermal variations and aging issues of the emerging devices are not included in this paper, but worth investigation in future work. Challenges with interfacing the emerging devices with silicon electronics should also be tackled, as many peripheral circuits are still expected to utilize CMOS technologies due to cost-effectiveness and, sometimes, performance or reliability concerns. Other potential challenges include better testing and variation characterization methods, specialized design automation tools for emerging technologies, etc.

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