Yuyang Wang

Columbia Nano Initiative, Columbia University
530 West 120th St, New York, NY 10027
+1 (781) 428-0408 yw3831@columbia.edu wangyy.phd

Research Interests

My research centers on enabling the design of system connectivity that is ultra high-bandwidth, energy-efficient, and adaptable in today's data-driven world. Tackling the significant communication bottlenecks found in modern distributed computing infrastructures, exacerbated by data-intensive AI and machine learning workloads, I am committed to designing—as well as democratizing the design process for—scalable architectures that maximize the capabilities of integrated silicon photonics, bridging communication and computation. With a deeper integration of photonics within computing sockets, I envision a paradigm shift in computing architectures that promises unparalleled interconnection bandwidth density, versatility, and functionalities.

Current Appointment

Columbia University in the City of New York — New York, NY, USA
Postdoctoral Research Scientist, Columbia Nano Initiative — 2021–Present

- Mentored by Prof. Keren Bergman

Education

University of California, Santa Barbara — Santa Barbara, CA, USA
Ph.D. in Electrical and Computer Engineering — 2018–2021

- Co-advised by Prof. Kwang-Ting Cheng and Prof. John E. Bowers

University of California, Santa Barbara — Santa Barbara, CA, USA
M.S. in Electrical and Computer Engineering — 2015–2018

Tsinghua University — Beijing, China
B.Eng. in Electronic Engineering — 2011–2015

Professional Experience

Semiconductor Research Corporation (SRC) Research Scholars Program
Research Scholar, Center for Ubiquitous Connectivity (CUbiC) under SRC JUMP 2.0 — 2023–Present

- Contributed to the writing and visualization of the proposal that led to the award of $35M JUMP 2.0 grant for the CUbiC Center
- Co-led the CUbiC Scholar Leadership Council to organize monthly workshops with industry liaisons

Hong Kong University of Science and Technology — Hong Kong SAR, China
Postgraduate Visiting Intern, Department of Electrical and Computer Engineering — Aug. 2019–Dec. 2019

Cadence Design Systems, Inc. — San Jose, CA, USA
Design Engineering Intern - Photonics, Custom IC & PCB Group — Jun. 2018–Sep. 2018

Rice University — Houston, TX, USA
Student Intern, Department of Electrical and Computer Engineering — Jul. 2014–Sep. 2014

Publications

Book Chapter

B1 **Y. Wang**, Z. Zhang, J. E. Bowers, and K.-T. Cheng, "Silicon photonics optical interconnects for data-centric artificial intelligence applications: A design automation perspective," in *Frontiers of Electronic Design (FED)*, A. Iranmanesh, Ed., in press, Cham: Springer International Publishing.

Refereed Journal Articles

J1 A. James, A. Rizzo, **Y. Wang**, A. Novick, S. Wang, R. Parsons, K. Jang, M. Hattink, and K. Bergman, "Process Variation-Aware Compact Model of Strip Waveguides for Photonic Circuit Simulation," *Journal of Lightwave Technology*, pp. 1–14, 2023. doi 10.1109/JLT.2023.3238847.

J2 A. Novick, A. James, L. Y. Dai, Z. Wu, A. Rizzo, S. Wang, **Y. Wang**, M. Hattink, V. Gopal, K. Jang, R. Parsons, and K. Bergman, "High-bandwidth density silicon photonic resonators for energy-efficient optical interconnects," *Applied Physics Reviews*, vol. 10, no. 4, p. 041 306, Nov. 2023. doi 10.1063/5.0160441.

J3 Z. Wu, L. Y. Dai, **Y. Wang**, S. Wang, and K. Bergman, "Flexible silicon photonic architecture for accelerating distributed deep learning," *Journal of Optical Communications and Networking*, 2023, to appear.

J4 **Y. Wang**, P. Sun, J. Hulme, M. A. Seyedi, M. Fiorentino, R. G. Beausoleil, and K.-T. Cheng, "Energy Efficiency and Yield Optimization for Optical Interconnects via Transceiver Grouping," *Journal of Lightwave Technology*, vol. 39, no. 6, pp. 1567–1578, Mar. 2021. doi 10.1109/JLT.2020.3039489.

J5 Z. Zhang, R. Wu, **Y. Wang**, C. Zhang, E. J. Stanton, C. L. Schow, K.-T. Cheng, and J. E. Bowers, "Compact Modeling for Silicon Photonic Heterogeneously Integrated Circuits," *Journal of Lightwave Technology*, vol. 35, no. 14, pp. 2973–2980, Jul. 2017. doi 10.1109/JLT.2017.2706721.

Refereed Conference Proceedings

C1 A. Novick, M. Hattink, A. Rizzo, **Y. Wang**, V. Gopal, S. Wang, R. Parsons, and K. Bergman, "Integrated photonic resonant modulator-based equalization and optimization for DWDM," in *Optical Fiber Communication Conference (OFC) 2024*, to appear, Optica Publishing Group, 2024.

C2 S. Wang, **Y. Wang**, X. Meng, K. Hosseini, T. T. Hoang, and K. Bergman, "Automated tuning of ring-assisted MZI–based interleaver for DWDM systems," in *Optical Fiber Communication Conference (OFC) 2024*, to appear, Optica Publishing Group, 2024.

C3 Z. Wu, R. Parsons, S. Wang, **Y. Wang**, and K. Bergman, "Wavelength reconfigurable transceiver for multi-interface compute accelerator networks," in *Optical Fiber Communication Conference (OFC) 2024*, to appear, Optica Publishing Group, 2024.

C4 G. Michelogiannakis, Y. Arafa, B. Cook, L. Y. Dai, A.-H. Hameed Badawy, M. Glick, **Y. Wang**, K. Bergman, and J. Shalf, "Efficient Intra-Rack Resource Disaggregation for HPC Using Co-Packaged DWDM Photonics," in *2023 IEEE International Conference on Cluster Computing (CLUSTER)*, Santa Fe, NM, USA: IEEE, Oct. 2023, pp. 158–172. doi 10.1109/CLUSTER52292.2023.00021.

C5 S. Wang, A. Novick, A. Rizzo, R. Parsons, S. Sanyal, K. J. McNulty, B. Y. Kim, Y. Okawachi, **Y. Wang**, A. Gaeta, M. Lipson, A. Gaeta, M. Lipson, and K. Bergman, "Integrated, Compact, and Tunable Band-Interleaving of a Kerr Comb Source," en, in *CLEO 2023*, San Jose, CA: Optica Publishing Group, 2023, STh3J.6. doi 10.1364/CLEO_SI.2023.STh3J.6.

C6 **Y. Wang**, S. Wang, A. Novick, A. James, R. Parsons, A. Rizzo, and K. Bergman, "Dispersion-Engineered and Fabrication-Robust SOI Waveguides for Ultra-Broadband DWDM," en, in *Optical Fiber Communication Conference (OFC) 2023*, San Diego California: Optica Publishing Group, 2023, Th3A.4. doi 10.1364/OFC.2023.Th3A.4.

C7 A. James, **Y. Wang**, A. Rizzo, and K. Bergman, "Flexible, Process-Aware Compact Model of Effective Index in Silicon Waveguides for Commercial Foundries," in *2022 International Conference on Numerical Simulation of Optoelectronic Devices (NUSOD)*, Turin, Italy: IEEE, Sep. 2022, pp. 173–174. doi 10.1109/NUSOD54938.2022.9894784.

C8 **Y. Wang** and K.-T. Cheng, "Traffic-Adaptive Power Reconfiguration for Energy-Efficient and Energy-Proportional Optical Interconnects," in *2021 IEEE/ACM International Conference On Computer Aided Design (ICCAD)*, Munich, Germany: IEEE, Nov. 2021, pp. 1–9. doi 10.1109/ICCAD51958.2021.9643475.

C9 **Y. Wang**, J. Hulme, P. Sun, M. Jain, M. A. Seyedi, M. Fiorentino, R. G. Beausoleil, and K.-T. Cheng, "Characterization and Applications of Spatial Variation Models for Silicon Microring-Based Optical Transceivers," in *2020 57th ACM/IEEE Design Automation Conference (DAC)*, San Francisco, CA, USA: IEEE, Jul. 2020, pp. 1–6. doi 10.1109/DAC18072.2020.9218608.

C10 **Y. Wang** and K.-T. Cheng, "Task Mapping-Assisted Laser Power Scaling for Optical Network-on-Chips," in *2019 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Westminster, CO, USA: IEEE, Nov. 2019, pp. 1–6. doi 10.1109/ICCAD45719.2019.8942146.

C11 **Y. Wang**, M. A. Seyedi, J. Hulme, M. Fiorentino, R. G. Beausoleil, and K.-T. Cheng, "Bidirectional tuning of microring-based silicon photonic transceivers for optimal energy efficiency," in *Proceedings of the 24th Asia and South Pacific Design Automation Conference*, Tokyo Japan: ACM, Jan. 2019, pp. 370–375. doi 10.1145/3287624.3287649.

C12 **Y. Wang**, M. A. Seyedi, R. Wu, J. Hulme, M. Fiorentino, R. G. Beausoleil, and K.-T. Cheng, "Energy-efficient channel alignment of DWDM silicon photonic transceivers," in *2018 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, Dresden, Germany: IEEE, Mar. 2018, pp. 601–604. doi 10.23919/DATE.2018.8342079.

C13 R. Wu, M. A. Seyedi, **Y. Wang**, J. Hulme, M. Fiorentino, R. G. Beausoleil, and K.-T. Cheng, "Pairing of microring-based silicon photonic transceivers for tuning power optimization," in *2018 23rd Asia and South Pacific Design Automation Conference (ASP-DAC)*, Jeju: IEEE, Jan. 2018, pp. 135–140. doi 10.1109/ASPDAC.2018.8297295.

C14 R. Wu, **Y. Wang**, Z. Zhang, C. Zhang, C. L. Schow, J. E. Bowers, and K.-T. Cheng, "Compact modeling and circuit-level simulation of silicon nanophotonic interconnects," in *Design, Automation & Test in Europe Conference & Exhibition (DATE), 2017*, Lausanne, Switzerland: IEEE, Mar. 2017, pp. 602–605. doi 10.23919/DATE.2017.7927057.

C15 A. Ghofrani, M. A. Lastras-Montaño, **Y. Wang**, and K.-T. Cheng, "In-place Repair for Resistive Memories Utilizing Complementary Resistive Switches," in *Proceedings of the 2016 International Symposium on Low Power Electronics and Design*, San Francisco Airport CA USA: ACM, Aug. 2016, pp. 350–355. doi 10.1145/2934583.2934590.

C16 C. Xu, F. X. Lin, **Y. Wang**, and L. Zhong, "Automated OS-level Device Runtime Power Management," in *Proceedings of the Twentieth International Conference on Architectural Support for Programming Languages and Operating Systems*, Istanbul Turkey: ACM, Mar. 2015, pp. 239–252. doi 10.1145/2694344.2694360.

Invited Conference Papers

I1 **Y. Wang**, S. Wang, R. Parsons, A. Novick, V. Gopal, K. Jang, A. Rizzo, C.-P. Chiu, K. Hosseini, T. T. Hoang, S. Shumarayev, and K. Bergman, "Silicon photonics chip I/O for ultra high-bandwidth and energy-efficient die-to-die connectivity," in *2024 IEEE Custom Integrated Circuits Conference (CICC)*, to appear, IEEE, 2024.

I2 **Y. Wang**, A. Novick, R. Parsons, S. Wang, K. Jang, A. James, M. Hattink, V. Gopal, A. Rizzo, C.-P. Chiu, K. Hosseini, T. T. Hoang, and K. Bergman, "Scalable architecture for sub-pJ/b multi-Tbps comb-driven DWDM silicon photonic transceiver," in *Next-Generation Optical Communication: Components, Sub-Systems, and Systems XII*, G. Li, K. Nakajima, and A. K. Srivastava, Eds., San Francisco, United States: SPIE, Mar. 2023, p. 55. doi 10.1117/12.2649506.

I3 **Y. Wang**, L. Shao, M. A. Lastras-Montano, and K.-T. Cheng, "Taming Emerging Devices' Variation and Reliability Challenges with Architectural and System Solutions [Invited]," in *2019 IEEE 32nd International Conference on Microelectronic Test Structures (ICMTS)*, Kita-Kyushu City, Fukuoka, Japan: IEEE, Mar. 2019, pp. 90–95. doi 10.1109/ICMTS.2019.8730924.

Under Review and In Preparation

P1 **Y. Wang**, S. Wang, R. Parsons, S. Sanyal, A. Novick, A. Rizzo, K. Jang, V. Gopal, K. J. McNulty, B. Y. Kim, Y. Okawachi, C.-P. Chiu, K. Hosseini, T. T. Hoang, S. Shumarayev, M. Lipson, A. Gaeta, and K. Bergman, "Scalable co-packaged dwdm silicon photonics chip i/o driven by microresonator Kerr frequency combs," *Nature Communications Physics*, 2024, invited, in preparation.

Talks and Presentations

Invited talk SPIE Photonics West, San Francisco, CA, USA — Jan. 2023

Scalable Architecture for Sub-pJ/b Multi-Tbps Comb-Driven DWDM Silicon Photonic Transceiver

Poster Ph.D. Forum, ACM/IEEE Design Automation Conference (DAC), online virtual event — Jun. 2020

Design and Optimization of Variation-Aware Runtime-Reconfigurable Optical Interconnects

Invited talk Optical/Photonic Interconnects for Computing Systems (OPTICS) workshop, Dresden, Germany — Mar. 2018

Optimal Pairing and Non-Uniform Channel Alignment of Microring-based Transceivers for Comb Laser-Driven DWDM Silicon Photonics

Invited talk ECE Departmental Seminar, Hong Kong University of Science and Technology, Hong Kong SAR, China — Jan. 2018

Variation-Aware Modeling and Design of Silicon Photonic Systems

Poster Optical/Photonic Interconnects for Computing Systems (OPTICS) workshop, Lausanne, Switzerland — Mar. 2017

Variation-Aware Modeling and Design of Nanophotonic Interconnects

Leadership

Center for Ubiquitous Connectivity (CUbiC) — SRC JUMP 2.0

- Co-led the CUbiC Scholar Leadership Council to organize monthly workshops with industry liaisons — 2023–Present
- Co-led the Socket-to-Socket Distributed AI/ML/HPC Fabric Platform (SoSFab) research task for system testbed development — 2023–Present

Columbia University in the City of New York — New York, NY, USA

- Led the photonic integrated circuit (PIC) team, supervised by Prof. Keren Bergman, under the DARPA CHIPS program — 2021-Present
- Co-led the design aggregation of a custom 300 mm full-wafer run with AIM Photonics involving multiple internal/external riders — 2023

Professional Service

Journal Reviewer

- Nature Nanotechnology
- IEEE Journal on Selected Areas in Communications
- IEEE Transactions on Computers
- IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems
- IEEE Transactions on Very Large Scale Integration (VLSI) Systems
- IEEE Access

Conference External Reviewer

– IEEE International Symposium on High-Performance Computer Architecture (HPCA) 2020

Textbook Translation

T1 C. Hawkins, J. Segura, and P. Zarkesh-Ha, *CMOS Digital Integrated Circuits: A First Course (Chinese Edition)*, trans. by **Y. Wang** and Y. Yin. China Machine Press, 2016, original work published by the Institution of Engineering and Technology (IET) in 2013.

T2 S. Kundu and A. Sreedhar, *Nanoscale CMOS VLSI Circuits: Design for Manufacturability (Chinese Edition)*, trans. by **Y. Wang** and W. Xie. China Science Publishing, 2014, original work published by McGraw-Hill Education in 2010.

Teaching Experience

Columbia University in the City of New York New York, NY, USA

Guest Lecturer Spring 2023 ELEN 9403: Seminar in Photonics (Graduate-level)

University of California, Santa Barbara Santa Barbara, CA, USA

Teaching Assistant Winter 2019 ECE 153B: Sensor & Peripheral Interface Design (Undergraduate-level)

Student Mentoring

Songli Wang
Ph.D. Student at Columbia University
Scalable link architectures, automated post-fabrication tuning
Resulting joint publication(s): [C2], [I1], [P1], [I2]

Zhenguo Wu
Ph.D. Student at Columbia University
Reconfigurable architecture for optically connected systems
Resulting joint publication(s): [C3], [J3]

Robert Parsons
Ph.D. Student at Columbia University
Compact modeling of silicon photonic devices and circuits
Resulting joint publication(s): [I1], [I2]

Aneek E. James
Ph.D. Student at Columbia University, now with Draper Laboratory
Wafer-scale process variation extraction and characterization
Resulting joint publication(s): [J1], [C7]

Kaylx Jang
Ph.D. Student at Columbia University
Dispersion-engineered and fabrication-robust (de-)interleavers
Resulting joint publication(s): [C6]

Max Haimowitz
Ph.D. Student at Columbia University
Scripted and automated large-scale silicon photonics chip layout
> 80 mm²/reticle fully-scripted layout on a 300 mm full-wafer run

Awards and Honors

Graduate Fellowship, Department of Electrical and Computer Engineering, University of California, Santa Barbara, CA, USA 2015

Outstanding Thesis Award, Department of Electronic Engineering, Tsinghua University, Beijing, China 2015

Scholarship for Sports Excellence, Department of Electronic Engineering, Tsinghua University, Beijing, China 2014

References

Ⓐ: from academia; Ⓘ: from industry

Ⓐ **Keren Bergman**
Charles Batchelor Professor of Electrical Engineering
Columbia University in the City of New York
bergman@ee.columbia.edu

Ⓐ **Kwang-Ting Cheng**
Vice-President for Research and Development, Chair Professor
Hong Kong University of Science and Technology
timcheng@ust.hk

Ⓐ **John E. Bowers**
Director of Institute for Energy Efficiency, Distinguished Professor
University of California, Santa Barbara
jbowers@ucsb.edu

Ⓘ **Raymond G. Beausoleil**
Senior Fellow and Senior Vice President
Hewlett Packard Enterprise
ray.beausoleil@hpe.com

Ⓐ Yuan Xie
Chair Professor
Hong Kong University of Science and Technology
yuanxie@ust.hk

Ⓘ Kaveh Hosseini
Technical Lead, Photonics Co-Packaging Architect
Intel Corporation
kaveh.hosseini@intel.com

Ⓘ M. Ashkan Seyedi
Principal, Silicon Photonics Products
Nvidia Corporation
mseyedi@nvidia.com